Patent
Attorney's Docket No. 017750-506

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	
Robert J. MARTIN	Group Art Unit: 2878
Application No.: 09/666,301	Examiner: Timothy J. MORAN
Filed: 21 September 2000	Appeal No. *Unassigned*
For: TWO COLOR QUANTUM WELL FOCAL PLANE ARRAYS	Confirmation No.: 8409

NEW BRIEF FOR APPELLANT

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Brief is a new brief in response to the Notification of Non-Compliance with 37 C.F.R. § 1.192(c) mailed on 03 June 2003 (Paper No. 11).

No fee payments are required for this submission, because payment covering the $320.00 (1402) Government fee for an Appeal Brief was previously filed on 13 May 2003, and this new brief is being filed within one month or 30 days from the 03 June 2003 mailing date of Paper No. 11. Accordingly, no additional payment is required for this submission. Two extra copies of this new brief are filed herewith.

This appeal is from the decision of the Primary Examiner dated (Paper No. 6), finally rejecting claims 7 and 9-10, which are reproduced as an Appendix to this brief.

I. Real Party in Interest

The present application is assigned to Lockheed Martin Corporation, a corporation organized under and pursuant to the laws of Maryland, U.S.A., and having its principal place of business at 6801 Rockledge Drive, Bethesda, Maryland, U.S.A. 20817.

II. Related Appeals and Interferences

The Appellant's legal representative, or assignee does not know of any other appeal or interferences which will affect or be directly affected by or have bearing on the Board's decision in the pending appeal.

III. Status of Claims

Claims 7 and 9-10 are pending. Claims 1-6, 8 and 11 are canceled. Claims 7 and 9-10 stand finally rejected under 35 U.S.C. § 112, 1st paragraph pursuant to the Office Action mailed 14 June 2002. The rejection of each of Claims 7 and 9-10 is hereby appealed.

IV. Status of Amendments

An Amendment was filed on 13 May 2003 (an even date with the filing of this Appeal Brief). The 13 May 2003 Amendment amends the specification as requested by the Examiner in the 14 June 2003 Final Office Action, and cancels Claims 1-6, 8 and 11.

V. Summary of the Invention

Exemplary embodiments of the present invention are directed to a readout circuit that receives charges from a photodector, for example in infrared photodetector. The circuit varies an integration time of moving charges from the photodetector, and includes a first charge well for receiving moving charges from the photodetector, at least one additional charge well, and a mechanism for selectively switching the at least one additional charge well in parallel with the first charge well to vary the integration time of the moving charges. An exemplary circuit in accordance with the present invention is shown in Figure 2 of the present application.

Employing two or more charge wells in the read out circuit of Figure 2 to vary the integration time, improves the gain and dynamic range of the read out circuit. At long ranges with faint targets, the number of volts per electron becomes a significant factor and signal to noise ratios thus become critical. As a hot target gets closer, the need changes from the need for maximizing the noise to avoiding saturation due to the very large number of target electrons rapidly filling the charge well. The exemplary read out circuit shown in Fig. 2 and encompassed by the present claims solves this problem by augmenting the integration time through a change in the charge well capacitance. This is done via the two charge well capacitances C_{w1} **200** and C_{w2} **205**. Application of a gain switching voltage GN **240** switches in the smaller charge well capacitance C_{w2} **205** to add another twenty decibels of dynamic range to the system's performance. A high total dynamic range performance of 128 decibels can thus be realized (68 dB small well, 40 dB integration time modulation, and 20 dB well change). See, for example, the originally filed specification at page 9, line 19 to page 10, line 4.

VI. The Issues

The issue on appeal is whether claims 7 and 9-10 are unpatentable under the enablement requirement of 35 U.S.C. § 112, 1st paragraph.

VII. Grouping of Claims

Claims 7 and 9 stand or fall together. Claim 10 stands separately.

VIII. Argument

Claim 10 stands separately because it is a method claim and the application is not required to recite structure corresponding to the actions recited in a method claim. In contrast, Claims 7 and 9 are apparatus claims. Claim 10 has different scope and character than Claims 7 and 9, and therefore stands separately from Claims 7 and 9. Furthermore, Claim 7 recites *selectively switching*, whereas Claim 10 recites *selectively varying*. The recitations are different and should be separately evaluated.

In the Office Action, the Examiner rejects Claims 1-11 under 35 U.S.C. § 112, 1st paragraph on grounds the claims are not enabled by the application as originally filed. This rejection is incorrect.

The originally filed specification at page 9, line 23 to page 10, line 2 states:

> *"As a hot target gets closer, the need changes from the need for maximizing the noise to avoiding saturation due to the very large number of target electrons rapidly filling the charge well. The exemplary read out circuit of Fig. 2 solves this problem by augmenting the integration time through a change in the charge well capacitance. This is illustrated in Figure 4 [sic] by the use of the two charge well capacitances C_{w1} 200 and C_{w2} 205. Application of a gain switching voltage GN 240 switches in the smaller charge well capacitance C_{w2} 205 to add another twenty decibels of dynamic range to the system's performance."*

This clearly teaches that the charge well fill rate increases as the target gets closer, and based on the fill rate ("... *the very large number of target electrons rapidly filling the charge well*") the second charge well capacitance is switched into parallel connection with the first charge well capacitance to avoid saturation. Accordingly, the originally filed application teaches a *selectively switching the at least one additional charge well in parallel with the first charge well to vary the integration time of the moving charges, based on a rate at which the moving charges fill the first charge well*, as recited in Claim 7, and teaches *selectively varying said integration capacitance to vary the integration time of said moving*

charges, based on a rate at which the moving charges fill the first charge well, as recited in Claim 10.

Subtleties of capacitor saturation were well known in the art at the time of the invention, as well as methods of gauging the charge well fill rate. Thus, given the disclosure in the specification at page 8, lines 23-25 regarding monitoring the output of the read out circuit of Figure 2 at the end of a time interval, and given the state of the art at the time of the invention, the person of ordinary skill in the art at the time of the invention would have been able to make and use the claimed invention. In addition, Applicant respectfully submits that methods for detecting and/or avoiding "saturation" in multi-pixel or detector arrays, for example by discerning excessively bright and excessively homogenous outputs from pixels or detectors in the array, were known in the art at the time of the invention, and therefore the person of ordinary skill at the time of the invention present application, would easily have applied such techniques or mechanisms to the disclosure of the present application to appropriately switch the second charge well capacitance into parallel connection with the first charge well capacitance.

Thus, the originally filed application enables pending Claims 7 and 9-10 and satisfies requirements of 35 U.S.C. § 112, 1st paragraph with respect to Claims 7 and 9-10.

IX. Conclusion

For at least the foregoing reasons, Appellant respectfully requests that the Examiner's rejection of claims 7 and 9-10 under § 112, 1st paragraph be REVERSED.

Respectfully submitted,

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APPENDIX A

The Appealed Claims

7. A circuit for varying the integration time of moving charges from a photodetector comprising:

a first charge well for receiving moving charges from a photodetector;

at least one additional charge well; and

means for selectively switching the at least one additional charge well in parallel with the first charge well to vary the integration time of the moving charges, based on a rate at which the moving charges fill the first charge well.

9. The circuit of claim 7, wherein each charge well comprises a capacitor.

10. A method of varying the integration time of moving charges from a photodetector comprising the steps of:

supplying moving charges from a photodetector to an integration capacitance; and

selectively varying said integration capacitance to vary the integration time of said moving charges, based on a rate at which the moving charges fill the first charge well.

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